Samit Shahnawaz Miftah

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Research Summary:

PhD researcher in Computer & Systems Engineering at RPI, advised by Prof. Kanad Basu, specializing in hardware security, verification, and AI for hardware design. Author of 10 peer-reviewed publications (5 as first author) at top IEEE/ACM venues including MICRO, DAC, HOST, and TCAD. Research spans hardware fuzzing (SymbFuzz, InterconFuzz), automated program repair (FlowFixer), LLM-based assertion generation (SpecGuard), security bug localization (RTL-Spec), and chiplet-based GPU architecture optimization. Two-time top-3 finisher at Hack@DAC and multiple award recipient at CSAW.

Education:

Rensselaer Polytechnic Institute – Computer & Systems Engineering, PhD — *August 2025 - Current*

The University of Texas at Dallas – Computer Engineering, PhD (GPA: 3.89/4.*00*) — *August 2022 - July 2025*

Bangladesh University of Engineering and Technology – Electrical and Electronic Engineering, BSc (GPA: 3.15/4.00) — *February 2015-April 2019*

Academic Achievements and Services:

1. 2nd and 3rd Place – Hack@DAC 2025 and 2024 respectively, one of the largest hardware security competitions at IEEE/ACM DAC.
2. 3rd Place and Finalist – AI Hardware Attack Challenge, CSAW 2025, 2023, and 2022 (Cyber Security Awareness Week, NYU Tandon).

Publications (7 Conference, 3 Journal):

1. **S. S. Miftah**, A. Srivastava, H. Kim, Shiyi Wei, and K. Basu, "SymbFuzz: Symbolic Execution Guided Hardware Fuzzing," 2025 58th IEEE/ACM International Symposium on Microarchitecture (MICRO), 2025.
2. **S. S. Miftah**, H. Kim, and K. Basu, "Interconfuzz: A fuzzing-based comprehensive NoC verification framework," 2025 62nd ACM/IEEE Design Automation Conference (DAC), 2025.
3. **S. S. Miftah**, S. Kundu, A. Mordahl, S. Wei and K. Basu, "RTL-Spec: RTL Spectrum Analysis for Security Bug Localization," 2024 IEEE International Symposium on Hardware Oriented Security and Trust (HOST), Tysons Corner, VA, USA, 2024.
4. **S. S. Miftah**, K. Raj, X. Meng, S. Ray and K. Basu, "System-on-Chip Information Flow Validation Under Asynchronous Resets," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), vol. 43, no. 9, pp. 2825–2838, Sept. 2024.
5. **S. S. Miftah**, A. Srivastava, H. Kim, and K. Basu, "Assert-O: Context-based assertion optimization using LLMs," in Proceedings of the Great Lakes Symposium on VLSI 2024, ser. GLSVLSI'24. ACM, 2024.
6. A. Srivastava, **S. S. Miftah**, H. Kim, D. Pal, and K. Basu, "PoSyn: Secure power side-channel aware synthesis," in IEEE Transactions on Very Large Scale Integration Systems (TVLSI), 2026.
7. A. Menon, **S. S. Miftah**, S. Kundu, S. Kundu, A. Raha, S. Banerjee, D. Mathaikutty, and K. Basu, "OpenAssert: Towards Secure Assertion Generation using Large Language Models," 2025 IEEE 43rd VLSI Test Symposium (VTS), 2025.
8. A. Menon, **S. S. Miftah**, S. Kundu, S. Kundu, A. Srivastava, A. Raha, G. Sonnenschein, S. Banerjee, D. Mathaikutty, and K. Basu, "Enhancing large language models for hardware verification: A novel SystemVerilog assertion dataset," ACM Transactions on Design Automation of Electronic Systems (TODAES), Aug. 2025.
9. **S. S. Miftah**, M. Towsif Abir, M. S. Hossain, A. Chakrabartty and M. S. Islam, "Image Processing Method for Measurement of Refractive Index," 2019 IEEE International Conference on Electrical, Computer and Communication Technologies (ICECCT), 2019.
10. M. T. Abir, L. Rahman, **S. S. Miftah**, S. Sarker, M. I. Al Imran and M. Shafiqul Islam, "Image Encryption and Decryption using Enigma Algorithm," 2019 IEEE International Conference on Electrical, Computer and Communication Technologies (ICECCT), 2019.

Selected Projects:

1. SpecGuard: Token-Efficient LLM-Based SVA Generation

- Challenge: LLM-based SVA generation collapses on large RTL due to token exhaustion, unstructured context, and frequent syntactic/semantic errors in generated assertions.
- Developed SpecGuard – distills RTL into AST skeletons and facts cards so the model's budget goes to assertion formulation, not design comprehension; achieves up to 987× higher functional coverage and 97% lower tokens-per-covered-event vs. state-of-the-art on 11 NVDLA/Coral NPU designs.

2. FlowFixer: Control-Flow-Based Automatic RTL Program Repair

- Challenge: Hardware repair remains manual despite verification tools – localization heuristics misfire, rule-based tools cannot generalize, and naive LLM repair hallucinates without CFG-level context.
- Developed FlowFixer – CFG/AST-driven bifurcated repair engine routes structural bugs to deterministic templates and complex flaws to a ReAct LLM agent; multi-tiered validation funnel with QoR scoring selects the minimal-area patch. Repairs 33% more bugs than RTL-Repair and 60% more than CirFix across 32 benchmarks.

3. CHoRD: Joint Scheduling and Data Placement for Chiplet-Based GPUs

- Challenge: Existing chiplet-GPU approaches optimize scheduling or placement independently, causing sustained inter-chiplet NUMA traffic that degrades DNN inference performance.
- Mentoring a graduate student developing CHoRD – a compiler-assisted, profile-guided framework for joint kernel scheduling and data placement; achieves 2.94× geo-mean speedup over round-robin and 1.66× over placement-only baseline across 9 CNN/transformer workloads.

Technical Skills:

Subjects	:	Hardware Security, Hardware Verification, Computer Architecture, VLSI Design.
Programming Languages	:	C/C++, Python, Scala, XML, TCL.
HDL	:	Verilog/SystemVerilog, Chisel, **Experience with** VHDL.
Tools	:	**Xilinx** – Vivado, Vitis HLS; **Cadence** – Virtuoso, Genus, Innovas, Xcelium, JasperGold; **Synopsys** – VCS, Design vision, Spyglass Lint; SymbiYosys, SMT-solver (Microsoft z3-Solver).
Technologies/Frameworks	:	Universal Verification Methodology **(UVM)**, Chipyard, Gem5, Linux, Git, LLM models (LangChain); Xilinx FPGA Boards, Raspberry Pi, Arduino.